Real-Time Simulation of a Ship Propulsion Multi-machine Power System

April 30, 2007
Rev 2 June 15, 2007
Executive Summary

The present document reports on the real-time simulation of a ship propulsion multi-machine system composed notably of 5 induction machine drives and 6 AC synchronous generators each with a 6-pulse diode rectifiers.

The document shows tests to validate that 1) the proposed network can be simulated on multi-core/multi-PCs real-time platform with the used of task-decoupling stublines models and 2) the induction machine PWM inverters can be simulated accurately in real-time with Time-Stamped Bridge model, from Opal-RT.

The multi-machine model has been simulated at 20 us on an 8-core PCs system using simplified generator models (fixed-voltage behind an inductance.) or detailed dynamic D-Q machine models and its regulators.

Tests have also show that larger time step (and therefore less cores) could be used because the model is still accurate in the 50-70 us time step range if the DC-AC converter PWM carrier frequency in below 2000 Hz.

A more complex models with very detailed controllers and PWM carrier frequency above 5000 Hz may require the used of 12 to 16 processor cores.

Consequently, OPAL-RT eMEGAsim parallel simulators use state-of-the-art technologies to accurately simulate very large and complex ship propulsion systems in off-line mode for faster-than-real-time applications and in real-time mode for HIL applications to test real control systems.

Finally, eMEGAsim is also very scalable and takes advantage of new multi-core processor technologies as they are available from major computer system vendors. This is a clear advantage over other real-time simulator suppliers that must design their own custom computer boards, which normally used processor technologies that are often 2 to 3 years old. On the other hand, OPAL-RT eMEGAsim uses off-the-self computer boards manufactured by several computer board makers supporting latest generation of INTEL and AMD processors as soon as their become available.

OPAL-RT eMEGAsim will also be soon compatible with SGI ALTIX XE super computer using that same off-the-self computer technology as standard eMEGAsim systems.

Using off-the-self (COTS) commercial computer systems designed and manufactured for the very large consumer and industrial markets, ensure that eMEGAsim computers will be easily upgradeable to the next generation computer systems that will become available over the next 10 to 20 years. As realized for our military customer in USA, EUROPE, JAPAN, INDIA and CHINA, this is a clear and very important advantage over custom made systems design for a very small niche market.
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Revision History

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1 System Description

1.1 Model description

The model is implemented using the Matlab/Simulink environment, the SimPowerSystem library as well as the ARTEMIS solver and IGBT converter models from Opal-RT exclusive blocksets. The ARTEMIS real-time solver is used in conjunction with real-time switching events compensated inverter bridges, which are optimized with real-time interpolation techniques to improve accuracy.

The modeled system, described in Fig.1, is mainly composed of two generation groups of four synchronous generators each and five induction machines drive loads interconnected by a DC bus.

In the first test series, each of the generation group includes four ideal sources behind R-L circuits rated 230V at a frequency of 60Hz. The AC voltage provided by each generator is rectified by a 6-pulse ideal diode rectifier with R-C snubbers and is isolated using an Yg-Y transformer of unary windings ratio. The diode rectifier that is used is the SPS Universal bridge model. The use of stublines is essential in order to get real-time performances because it produces decoupling of the underlying computational models. In order to lighten the calculation task of the two CPUs assigned to the generation groups, the system is therefore decoupled by one stubline at the end of each rectifier.

Every load component is a squirrel cage induction motor, rated 4 HP at 220V and 60 Hz, fed by a DC/AC converter, isolated with a unary windings ratio Y-D transformer. They are all rotating at constant speed hence mechanically coupled to an infinite mass. The three-phase, 2-level inverters are Time-Stamp Bridges from the RTE-Drive Blockset and are each gate-controlled by an RT-EVENT PWM generator (constant frequency modulation ratio and constant amplitude modulation ratio).

Short decoupling lines (stublines) simulate the smoothing reactors in order to provide a virtual separation of the subsystems (each subsystem is assigned to a single CPU). The model capacitors (C1 to C5) have large values and provide the smoothing and stabilization of the DC bus voltage.

A second series of test has been done by replacing the ideal sources by detailed D-Q models of synchronous machines and a simple control system demonstrating the capability of the simulator to simulate power swing with rotor frequency oscillations.

1.2 Real-time simulator configuration

Table 1 and 2 shows the hardware and software configuration of the RT-LAB real-time simulator used for the tests.
### Table 1. RT-LAB simulator hardware description

<table>
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<tr>
<th>Feature</th>
<th>Description</th>
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<tbody>
<tr>
<td>CPU type</td>
<td>2 XEON Quad-Core chips (8 CPU cores)</td>
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<tr>
<td>CPU speed</td>
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</tr>
<tr>
<td>RAM</td>
<td>2 Gbytes</td>
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<tr>
<td>Operating System</td>
<td>QNX 6.3.2 (32 bits)</td>
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<tr>
<td>I/O</td>
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<tr>
<td>Real-Time Performance</td>
<td>20 µs</td>
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### Table 2. Software package used in the tests

<table>
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<tr>
<th>Software Package</th>
<th>Version</th>
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<tbody>
<tr>
<td>RT-LAB</td>
<td>Version 8.1.1</td>
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<tr>
<td>ARTEMIS</td>
<td>Version 4.1</td>
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<tr>
<td>RT-EVENTS Blockset</td>
<td>Version 3.0.1</td>
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<tr>
<td>MATLAB</td>
<td>R14 sp1</td>
</tr>
<tr>
<td>SimPowerSystem</td>
<td>4.0</td>
</tr>
</tbody>
</table>
2 Test Series 1

2.1 Real-Time Simulation expected performance with ideal sources

The complete model simulates at a real-time step of 20 microseconds on an 8-core RT-LAB simulator. If a larger time step is to be used, fewer CPU cores are necessary for real-time simulation.
Fig. 1. Model simulated on RT-LAB using Ideal Source
2.2 Validation Tests with Ideal Sources

This section purpose is to validate the models and methods used to simulate the model in real-time. As already explained, the model presents some challenges in terms of real-time simulation capability.

The most important challenges are:

1) The topological connection of a large number of switches at the rectifiers.
   Real-time simulation of switches systems is a challenge for real-time simulation because each time switches change position; it modifies the complete set of model equations to which the switch is connected. When the number of switches is too large, it becomes difficult to pre-computes all possibilities. The solution lies in the usage of ‘stublines’. Stublines are short lines with exactly 1 time step propagation delay. They can by inserted in model where an inductor or capacitor is present because they basically mimics the effects of a short PI line section.

2) The simulation of the induction machine inverters with high frequency PWM.
   High frequency PWM switching can cause bad accuracy problems in fixed step simulation schemes. Interpolation is necessary most of the time. Time-Stamped Bridges, from Opal-RT, provides accurate inverter simulation in real-time simulation by implementing fast interpolation techniques.

2.2.1 Test 1.1: Stubline model validation

This section compares the simulation of the model with and without stublines. The test consists on the application of a 3-phase fault for 0.2 seconds at the stator of induction machine #1.

Table 3 shows that the usage of stublines causes negligible errors at a time step of 50 us (that is 250% larger than the actual real-time step of 20 us) at the system level. This validates the capacity of the simulator to run large distributed simulations using stublines to decouple the model (multi-core or cluster-based). It also means that fewer cores could be used to simulate the system at 50 us and obtain accurate results.
Fig. 2. Induction motor voltages. With and without stublines.

Fig. 3. Induction machine currents. With and without stublines.
Fig. 4. Induction machine active power. With and without stublines.

Fig. 5. Induction machine reactive power. With and without stublines.

Table 3 Average error relative to the No-Stubline case

<table>
<thead>
<tr>
<th>Vab Machine 1</th>
<th>Ia Machine 1</th>
<th>P Machine 1</th>
<th>Q Machine 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.07%</td>
<td>0.05%</td>
<td>0.1%</td>
<td>0.2%</td>
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2.2.2 Test 1.2: Comparison of RTE-Drive Time-Stamp Bridge and SPS Universal Bridge at large time step (70 µs)

This section compares the Time Stamped Bridge (TSB) model from Opal-RT with the SimPowerSystem (SPS) model at 70 us. The SPS model is not designed to run simulation of inverter with high PWM to sampling frequency ratio. This ratio must usually be below 1/100 for acceptable precision. In this test, we use a time step of 70 us (sampling frequency is then 14.3 kHz) and carrier frequency of 500 Hz and this ratio is then 0.035, which is too high. The test is made with the stublines.

The typical effect of under-sampled PWM inverter simulation is the low-frequency jitter effect that can be observed very well in Fig.8 to Fig.11. This is a well-documented behaviour in the literature.

The limitation of SimPowerSystem is caused by the usage of a fixed step solver and is not a malfunction. Other packages like PSIM, PSpice, EMTP, and HYPERSIM have the same limitations: they must use very small time step or variable time step solvers to obtain accurate simulation of PWM inverters. The SimPowerSystem blockset is used by more than 5000 corporations worldwide as of 2006 and is an established reference.

Fig.6. Motor voltage. TSB vs. SPS at 70 us.
Fig. 7. Motor currents. TSB vs. SPS at 70 us.

Fig. 8. Active powers. TSB vs. SPS at 70 us.
Fig. 9. Zoom of active powers. TSB vs. SPS at 70 us

Fig. 10. Reactive powers. TSB vs. SPS at 70 us
2.2.3 Test 1.3: Comparison TSB results at 50 µs, 20 µs and 1 µs time steps.

This section test the ‘convergence’ of the TSB model from Opal-RT. Convergence means that a simulation model is getting more precise when the time step decreases. This property is notably used by variable-step variable order solver to control their time step.

We compare here the simulation results of Opal-RT TSB model at time step of 50, 20 and 1 us. The results show that the TSB model is convergent and as accurate at 50 us as using 1 us for the PWM frequency of 500 Hz.
Fig. 12. Motor voltages. TSB at 50, 20 and 1 us.

Fig. 13. Motor currents. TSB at 50, 20 and 1 us.
Fig. 14. Zoom of motor currents. TSB at 50, 20 and 1 us.

Fig. 15. Motor active powers. TSB at 50, 20 and 1 us.
3 Tests Series 2: Results with Detailed Synchronous Machine Models Instead of Ideal Voltage Sources

3.1 Details on modifications

In the second test series, each of the 8 ideal sources of the network shown on Fig.1 are replaced by 460 V/10.2 kVA synchronous machines (see Fig.17). Both field voltage and mechanical power values of the synchronous machines models are set externally through inputs. The field voltage value is controlled using the SimPowerSystem Excitation block and a standard PID controller is added to model a governor on the mechanical power. The models of the 5 load constant speed motors are replaced with the standard SimPowerSystem induction motor model. Mechanical torque applied on each motor is controlled with a simple function linking the mechanical torque with the rotor speed of the motor.
3.2 Validation Tests

3.2.1 Test 2.1 Fault on Motor 1
A 3-phase fault for 0.2 seconds is applied at the stator of the induction motor 1. The next figure presents motor 1 voltage, current and speed during the fault.

Fig. 17. Synchronous machine used in model

Fig. 18. Induction motors stator currents

3.2.2 Test 2.2: Fault on DC line
The next figure presents motors speeds when a 100 ms fault is applied on the DC line.

Induction motors stator currents
Fig.19. Induction motors stator currents

On the next figure, we observe the speed of the 4 first synchronous machines. In this case, a 0.1 seconds fault is applied on the DC line at 0.1 seconds.
Fig. 20. Synchronous machines speed

Fig. 21. DC line voltage and current
3.2.3 Test 2.2: Motor permanently removed during simulation

This test consists to delete the first motor during the simulation and observe the generators power. Each motor has a nominal power of 10200 VA.

In steady state with 5 motor loads, the generator power is around 0.285 pu (see Fig.22). When one of the motors is removed at 2.5 s, the power generated from each machine diminishes to a new stead-state value equivalent to the load of 4 motors.

![Power generated by one machine (pu)](image)

Fig.22. Generated power for one machine during the lost of one motor load

The generators speed slightly augments after one load removal at 3.5 seconds (see Fig.23). This is due to the generator governor control, which have a non-zero permanent relation between P and F. The generator speed behaves according to the governor controller implemented for this tests. This controller can be easily modified by users using SIMULINK blocks.

Finally, Fig.24 shows active power (in blue) and reactive power (in green) before, during and after the removal. Note that the initial oscillation of the P and Q sensors is due to the 6th harmonic caused by P and Q calculation. This can be filtered using a simple low-pass filter as done to compute results of Fig. 22.
Fig. 23. One machine speed in pu during the loss of one motor load

Fig. 24. Motor Electrical Power before and after being removed
4 Conclusions

The present document reports on the real-time simulation of multi-machine system composed notably of 5 induction machine drives and 8 AC-sources each with a 6-pulse diode rectifiers.

The main conclusions of this analysis are:

- The proposed network can be simulated on multi-core/multi-PCs real-time platform with the use of task-decoupling stubline models.
- The induction machine PWM inverters can be simulated accurately in real-time with Time-Stamped IGBT Inverter Bridge model developed by Opal-RT.
- The multi-machine model has been simulated at 20 us on an 8-core PCs system with simplified and complex machine models.
- Users can optimize and develop machine and power electronic controllers using standard SIMULINK blocks and Real-Time Workshop automatic code generators to implement real controllers.
- Tests have also show that larger time step (and therefore less cores) could be used because the model is still accurate in the 50-70 us time step range if the DC-AC converter PWM carrier frequency is below 2000 Hz.
- A more complex models with very detailed controllers and PWM carrier frequency above 5000 Hz may require the use of 12 to 16 processor cores.

From previous published work with MITSUBISHI, it was also demonstrated that detailed IGBT converter models with PWM carrier frequency up to 10 kHz can be simulated in normal INTEL processor cores. Very high-accuracy IGBT converter and machine models can also be implemented in FPGA cores to achieve sub-microsecond precision required for advanced controller design and tests. Users can implement their own models and control or use pre-compiled OPAL-RT models.

eMEGAsim can also take advantage of very accurate finite-element based real-time machine models that can be executed at high-speed (20 to 30 us) on normal INTEL or AMD processors or below 500 nanos using latest VIRTEX XILINX FPGA with user programmable tools. The number of processor core and IO channels required will however depend on the total system specification.

Consequently, OPAL-RT eMEGAsim parallel simulators use state-of-the-art technologies to accurately simulate very large and complex ship propulsion systems in off-line mode for faster-than-real-time applications and in real-time mode for HIL applications to test real control systems.

Finally, eMEGAsim is also very scalable and takes advantage of new multi-core processor technologies as they are available from major computer system vendors. This is a clear advantage over other real-time simulator suppliers that must design their own custom computer boards, which normally used processor technologies that are often 2 to 3 years old. On the other hand, OPAL-RT eMEGAsim uses off-the-self computer boards.
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